WHAT IS CLAIMED IS

1. A semiconductor device having a pad region and a circuit region, comprising:

a low-k dielectric film formed on a pad region and a circuit region a substrate, the low-k dielectric film having dielectric constant of 3 or less;

an insulating film formed in the low-k dielectric film of the pad region, the insulating film having higher strength than the low-k dielectric film;

multi-layer wirings formed in the insulating film of the pad region and in the low-k dielectric film of the circuit region; and

a bonding pad formed on a highest wiring of the multi-layer wirings of the pad region.

2. The semiconductor device according to claim 1, wherein sidewalls of the wiring formed in the pad region are surrounded by the insulting film.

3. The semiconductor device according to claim 1, wherein the low-k dielectric film is an insulating film containing silicon, carbon, oxygen and hydrogen, or a polymer film containing hydrogen and carbon.

4. A semiconductor device having a pad region and a circuit region, comprising:

multi-layer low-k dielectric films formed on a pad region and a circuit region a substrate, each of the multi-layer low-k dielectric films having dielectric constant of 3 or less;

insulating films formed in each of the multi-layer low-k dielectric films of the pad region, each of the insulating films having higher strength than the low-k dielectric film;

wirings formed in each of the insulating films of the pad region and in each of the low-k dielectric films of the circuit region; and

a bonding pad formed on a highest wiring of the wirings of the pad region.

5. The semiconductor device according to claim 4, wherein sidewalls of the wirings formed in the pad region are surrounded by the insulting films.

6. A method for manufacturing a semiconductor device having a pad region and a circuit region, comprising:

forming a low-k dielectric film on an entire surface of a substrate, the low-k dielectric film having dielectric constant of 3 or less;

forming an opening in the low-k dielectric film of the pad region;

forming a first insulating film having higher strength than the low-k dielectric film in the opening; and

forming wirings in the first insulating film of the pad region and in the low-k dielectric film of the circuit region using a damascene process.

7. The manufacturing method according to claim 6, wherein the forming an opening includes:

forming second insulating film on the low-k dielectric film;

forming a resist pattern on the second insulating film; and

patterning the second insulating film and the low-k dielectric film using the resist pattern as mask, and

wherein the first insulating film is formed so that a surface of the first insulating film is higher than a surface of the low-k dielectric film and is lower than a surface of the resist pattern.

8. The manufacturing method according to claim 6, wherein, in the forming a first insulating film, a silicon oxide film is formed using a liquid-phase deposition method.

9. The manufacturing method according to claim 6, multi-layer wirings are formed by repeating the forming a low-k dielectric film, forming an opening, forming a first insulating film and forming wirings, and

wherein a bonding pad is formed on a highest wiring of the multi-layer wirings of the pad region.